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Sheet 1 of 1

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| Application Number | 10/627,056 |
| Filing Date | July 25, 2003 |
| First Named Inventor | Daniel J. Smith |
| Art Unit | 2825 |
| Examiner Name | Siek, Vuthe |
| Attorney Docket Number | 003921.00151 |

NON PATENT LITERATURE DOCUMENTS

| Examiner Initials * | Cite No. | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
|------------------------|-------------|--|----------------|
| VS | | T. HUBING et al., Preliminary Embedded Capacitance Measurement Results, NCMS Embedded Capacitance Project, 10/23/99, 25 pp. | |
| VS | | TODD HUBING et al., Power Bus Noise Reduction Using Power Islands in Printed Circuit Board Designs, University of Missouri-Rolla Electromagnetic Compatibility Laboratory, November 11, 1999, 11 pp. | |
| VS | | TODD HUBING, Prof., University of Missouri-Rolla, PWB Power Bus Structures: Theory and Design, University of Missouri-Rolla Electromagnetic Compatibility Laboratory, IEEE EMC Society Rocky Mountain Chapter, November 11, 1999, 24 pp. | |
| VS | | ISTVAN NOVAK et al., SUN Microsystems, Inc., Simulating Complex Power-Ground Plane Shapes With Variable-Size Cell SPICE Grids, Manuscript for the 11 th Topical Meeting on Electrical Performance of Electronic Packaging October 21-23, 2002, Monterey, CA | |
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| Examiner Signature | VUTHE SIEK | Date Considered | 7/14/05 |
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